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F0999 **PATENT**

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of: Chow et al.

Serial No.: 09/893,100

Filed: June 26, 2001

Group Art Unit: 2661

Before the Examiner: Wahba, Andrew W.

Title: COLLISION RECOVERY INTERFACE SUPPORT IN A HOME PHONELINE NETWORKING ALLIANCE MEDIA ACCESS CONTROLLER (HPNA MAC) OPERATING IN ACCORDANCE WITH AT LEAST TWO DIFFERENT DATA RATE STANDARDS

APPEAL BRIEF

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

I. REAL PARTY IN INTEREST

The real party in interest is Advanced Micro Devices, Inc., which is the assignee of the entire right, title and interest in the above-identified patent application.

CERTIFICATION UNDER 37 C.F.R. §1.8

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to Mail Stop Appeal Brief-Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on December 6, 2005.

Toni Stanley
Signature

Toni Stanley
(Printed name of person certifying)

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II. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to Appellants, Appellants' legal representative or assignee which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 1-18 are pending in the Application. Claims 1-18 stand rejected. Claims 1-18 are appealed.

IV. STATUS OF AMENDMENTS

Appellants have not submitted any amendments following receipt of the final rejection with a mailing date of September 19, 2005.

V. SUMMARY OF CLAIMED SUBJECT MATTER

In one embodiment of the present invention, a method for collision recovery interface support in a home phoneline networking alliance (HPNA) control chip, the method may comprise the step of providing transmit data path logic to receive and transmit data packets within the HPNA control chip. Specification, page 4, line 1 – page 5, line 2; Figure 1, element 100; Figure 2, elements 202, 204. The method may further comprise consolidating the transmit data path logic to include a transmit state machine that handles interfacing the transmit data path logic to at least two separate collision recovery logic means of the HPNA control chip through a minimal number of generic interface signals. Specification, page 6, lines 1-22; Figure 2, elements 204, 206, 208; Figure 3, element 300.

In another embodiment of the present invention, the system as recited above may further comprise having the minimal number of interface signals further

comprising a GO signal from each separate collision recovery logic means. Specification, page 6, lines 1-22; Figure 2, elements 206, 208.

In another embodiment of the present invention, the system as recited in the second paragraph above, may further comprise having the at least two separate collision recovery logic means further comprise a BEB collision recovery means. Specification, page 5, lines 3-8; Specification, page 6, lines 1-22; Figure 2, element 208.

In another embodiment of the present invention, the system as recited in the third paragraph above, may further comprise having the at least two separate collision recovery logic means further comprise a DFPQ collision recovery means. Specification, page 5, lines 3-8; Specification, page 6, lines 1-22; Figure 2, element 206.

In another embodiment of the present invention, a system for collision recovery interface support in a home phoneline networking alliance (HPNA) control chip comprises at least two collision recovery means for providing collision recovery in the HPNA control chip according to at least two data rate standards. Specification, page 4, line 1 – page 5, line 8; Figure 1, element 100; Figure 2, elements 206, 208. The system may further comprise a transmit data path logic means including a transmit state machine that interfaces with the at least two collision recovery means through a minimal number of generic interface signals. Specification, page 6, lines 1-22; Figure 2, elements 204, 206, 208; Figure 3, element 300.

In another embodiment of the present invention, the system as recited above may further comprise having the minimal number of interface signals further comprising a GO signal from each separate collision recovery logic means. Specification, page 6, lines 1-22; Figure 2, elements 206, 208.

In another embodiment of the present invention, the system as recited in the second paragraph above, may further comprise having the at least two separate collision recovery logic means further comprise a BEB collision recovery means. Specification, page 5, lines 3-8; Specification, page 6, lines 1-22; Figure 2, element 208.

In another embodiment of the present invention, the system as recited in the third paragraph above, may further comprise having the at least two separate collision recovery logic means further comprise a DFPQ collision recovery means. Specification, page 5, lines 3-8; Specification, page 6, lines 1-22; Figure 2, element 206.

In another embodiment of the present invention, a home phone networking alliance (HPNA) network control chip capable of collision recovery interface support, the chip comprising a media independent interface (MII). Specification, page 4, lines 1-17; Figure 1, element 106. The chip may further comprise a physical layer (PHY). Specification, page 4, lines 1-17; Figure 1, element 110. The chip may further comprise a media access control (MAC) coupled between the MII and the PHY. Specification, page 4, lines 1-17; Figure 1, element 108. The MAC may further comprise at least two collision recovery means for providing collision recovery according to at least two data rate standards. Specification, page 4, line 1 – page 5, line 8; Figure 1, element 108; Figure 2, elements 206, 208. The MAC may further comprise a transmit data path logic means including a transmit state machine that interfaces with the at least two collision recovery means through a minimal number of generic interface signals. Specification, page 6, lines 1-22; Figure 1, element 108; Figure 2, elements 204, 206, 208; Figure 3, element 300.

In another embodiment of the present invention, the system as recited above may further comprise having the minimal number of interface signals further

comprising a GO signal from each separate collision recovery logic means, a new transmit signal, a transmit done signal, and a transmit priority indicator from the transmit data. Specification, page 6, lines 1-22; Figure 2, elements 206, 208.

In another embodiment of the present invention, the system as recited in the second paragraph above, may further comprise having the at least two separate collision recovery logic means further comprise a BEB collision recovery means. Specification, page 5, lines 3-8; Specification, page 6, lines 1-22; Figure 2, element 208.

In another embodiment of the present invention, the system as recited in the third paragraph above, may further comprise having the at least two separate collision recovery logic means further comprise a DFPQ collision recovery means. Specification, page 5, lines 3-8; Specification, page 6, lines 1-22; Figure 2, element 206.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1, 2, 3, 4, 8, 9, 10, 11 and 15 stand rejected under 35 U.S.C. §102(b) as being anticipated by Mills (U.S. Patent No. 5,991,303). Claims 5, 6, 7, 12, 13, 14, 16, 17 and 18 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Kakiuchi in view of Lu et al. (U.S. Patent No. 6,839,345) (hereinafter "Lu").

VII. ARGUMENT

A. Claims 1, 2, 3, 4, 8, 9, 10, 11 and 15 are not properly rejected under 35 U.S.C. §102(b) as being anticipated by Mills.

The Examiner has rejected claims 1, 2, 3, 4, 8, 9, 10, 11 and 15 under 35 U.S.C. §102(b) as being anticipated by Mills. Paper No. 5, page 2. Appellants respectfully traverse these rejections for at least the reasons stated below.

For a claim to be anticipated under 35 U.S.C. §102, each and every claim limitation must be found within the cited prior art reference and arranged as required by the claim. M.P.E.P. §2131.

1. Claim 1 is not anticipated by Mills.

Appellants respectfully assert that Mills does not disclose "providing transmit data path logic to receive and transmit data packets within the HPNA control chip" as recited in claim 1. The Examiner cites column 6, lines 16-21 of Mills as disclosing the above-cited claim limitation. Paper No. 5, page 2. Appellants respectfully traverse and assert that Mills instead discloses a line driver/receiver circuit that is coupled to communicate information with a font end multiplexer circuit. Column 6, lines 16-18. Mills further discloses that the select input of the front end multiplexer circuit is controlled by a control signal in a bus generated by an auto-negotiation circuit. Column 6, lines 18-21. There is no language in the cited passage that discloses an HPNA control chip. Appellants performed a search of the term "HPNA" and were unable to identify the term "HPNA" or any variation thereof. Further, there is no language within the cited passage that discloses providing transmit data path logic to receive data packets within a HPNA control chip. Neither is there any language within the cited passage that discloses providing transmit data path logic to transmit data packets within a HPNA control chip. Thus, Mills does not disclose all of the limitations of claim 1, and thus Mills does not anticipate claim 1. M.P.E.P. §2131.

In response to Appellants' above argument, the Examiner asserts that line driver/receiver 250 of Mills discloses a transmit data path logic. Paper No. 5, page 6. Further, the Examiner cites column 6, lines 13-14 and 16-21 of Mills as disclosing an HPNA chip. Paper No. 5, page 6. Further, the Examiner asserts that a twisted pair wire is well known and then concludes that Mills effective discloses an HPNA control

chip since Mills utilizes an Ethernet 802.xx standard. Paper No. 5, page 6. Appellants respectfully contend that Mills does not disclose the above-cited claim limitation.

While a twisted pair wire may be well known and Mills discloses using the Ethernet communication protocol (IEEE 802.3 standard) (column 1, lines 8-10), the Examiner has not provided a basis in fact and/or technical reasoning to support the conclusion that since Mills discloses using the IEEE 802.3 standard and a twisted pair wire may be well known that Mills effectively discloses an HPNA control chip. An HPNA control chip is based on the specifications of the Home Phoneline Networking Alliance (HPNA) that achieves communication among multiple computers within a home environment. Specification, page 1, lines 12-14. The HomePNA, as it is commonly called, is regarded generally as easy to install, inexpensive and fast, without requiring any additional wiring, since the phone lines that are already present in the home are used. Specification, page 1, lines 14- 17. HomePNA operates using a method known as frequency division multiplexing, which allows voice and data to travel on the same wires without interfering with each other, since a standard phone line has enough room to support voice, a high-speed DSL modem and a home phone line network. Specification, page 1, line 17 – page 2, line 2. Mills, on the other hand, discloses a multi-communication rate switching physical device for a port of a mixed communication rate Ethernet repeater network. Abstract. An Ethernet repeater takes a signal from one Ethernet cable and repeats it onto another Ethernet cable. See definition of "Ethernet repeater" at http://en.wikipedia.org/wiki/10/100_Ethernet. Further, the IEEE 802.3 standard is a collection of IEEE standards defining the physical layer and the transport layer of the wired. See definition of "IEEE 802.3" at http://en.wikipedia.org/wiki/IEEE_802.3. Hence, it is clear that Mills, which discloses a device used for a port of an Ethernet repeater network, is not related to HPNA networks.

The Examiner must provide a basis in fact and/or technical reasoning to support the conclusion that since Mills discloses using the IEEE 802.3 standard and a twisted pair wire may be well known that Mills effectively discloses an HPNA control chip. *Ex parte Levy*, 17 U.S.P.Q.2d 1461, 1464 (Bd. Pat. App. & Inter. 1990). That is, the Examiner must provide extrinsic evidence that must make clear that since Mills discloses using the IEEE 802.3 standard and a twisted pair wire may be well known that Mills effectively discloses an HPNA control chip, and that it be so recognized for persons of ordinary skill. *In re Robertson*, 169 F.3d 743, 745, 49 U.S.P.Q.2d 1949, 1950-51 (Fed. Cir. 1999). Since the Examiner has not provided such evidence, the Examiner has not presented a *prima facie* case of anticipation in rejecting claim 1. M.P.E.P. § 2131.

Furthermore, the additional passage cited by the Examiner (column 6, lines 10-12 of Mills) does not disclose "providing transmit data path logic to receive and transmit data packets within the HPNA control chip" as recited in claim 1. Instead, Mills discloses a media access controller that can construct a packet of information based on the recovered bits. Column 6, lines 10-12. There is no language in the cited passage that discloses the above-cited claim limitation. Thus, Mills does not disclose all of the limitations of claim 1, and thus Mills does not anticipate claim 1. M.P.E.P. §2131.

Appellants further assert that Mills does not disclose "consolidating the transmit data path logic to include a transmit state machine that handles interfacing the transmit data path logic to at least two separate collision recovery logic means of the HPNA control chip through a minimal number of generic interface signals" as recited in claim 1. As understood by the Appellants, the Examiner cites column 6, lines 16-21 and column 7, lines 1-5 of Mills as disclosing the above-cited claim limitation. Paper No. 5, page 2. Appellants respectfully traverse. As stated above, Mills instead discloses a line driver/receiver circuit that is coupled to communicate

information with a font end multiplexer circuit. Column 6, lines 16-18. Mills further discloses that the select input of the front end multiplexer circuit is controlled by a control signal in a bus generated by an auto-negotiation circuit. Column 6, lines 18-21. Mills further discloses that the select input of the back end multiplexer is controlled by the control bus that receives part of its signal from the result of the auto-negation circuit and part of its signal from a management interface circuit. Column 7, lines 1-5. There is no language in the cited passage that discloses consolidating a transmit data path logic to include a transmit state machine. Appellants performed a search of the phrase "state machine" in Mills and were unable to identify the phrase "state machine" or any variation thereof in Mills. Neither is there any language in the cited passage that discloses consolidating a transmit data path logic to include a transmit state machine that handles interfacing the transmit data path logic to at least two separate collision recovery logic means. Neither is there any language in the cited passage that discloses consolidating a transmit data path logic to include a transmit state machine that handles interfacing the transmit data path logic to at least two separate collision recovery logic means of a HPNA control chip. Neither is there any language in the cited passage that discloses consolidating a transmit data path logic to include a transmit state machine that handles interfacing the transmit data path logic to at least two separate collision recovery logic means of a HPNA control chip through a minimal number of generic interface signals. Thus, Mills does not disclose all of the limitations of claim 1, and thus Mills does not anticipate claim 1. M.P.E.P. §2131.

In response to the above argument, the Examiner cites element 250 of Mills as disclosing the transmit data path logic. Paper No. 5, page 7. The Examiner further cites elements 260 and 270 as well as column 6, lines 16-21 and column 7, lines 1-5 of Mills as disclosing a transmit state machine. Paper No. 5, page 7. The Examiner further cites column 6, lines 16-21 of Mills as disclosing interfacing the transmit data path logic. Paper No. 5, page 7. The Examiner further cites elements 210 and 212 as

disclosing two separate collision recovery logic means. Paper No. 5, page 7. The Examiner further cites elements 220 and 230 as disclosing a minimal number of generic interface signals. Paper No. 5, page 7. Appellants respectfully traverse the assertion that Mills discloses the above-cited claim limitation. Paper No. 5, page 7.

Mills instead discloses that the result of the auto-negotiation circuit 260 is used by the present invention to control both the front and back end multiplexers. Column 7, lines 13-16. Mills further discloses that auto-negotiation is performed between the auto-negotiation circuit 260 and an analogous auto-negotiation circuit 261 within adapter 280 in accordance with the IEEE 802.3 standard. Column 7, lines 16-19. Mills further discloses that the result of the auto-negotiation indicates whether adapter 280 supports 10 M or 100 M networking. Column 7, lines 19-21. Mills further discloses that the select input of the back end multiplexer is controlled by the control bus that receives part of its signal from the result of the auto-negotiation circuit and part of its signal from a management interface circuit 270. Column 7, lines 1-5. There is no language in Mills that discloses that the auto-negotiation circuit 260 and the management interface circuit 270 (Examiner asserts that elements 260 and 270 together disclose a transmit state machine) together handle interfacing the transmit data path logic (Examiner asserts that line driver/receiver 250 of Mills discloses a transmit data path logic) to at least two separate collision recovery logic means (Examiner asserts that elements 210 and 212 discloses collision recovery logic means) of the HPNA control chip through a minimal number of generic interface signals. Instead, auto-negotiation circuit 260 performs auto-negotiation to indicate whether adapter 280 supports 10 M or 100 M networking. Further, Mills instead discloses that a signal is used from the management interface circuit 270 to control the back end multiplexer. Thus, Mills does not disclose all of the limitations of claim 1, and thus Mills does not anticipate claim 1. M.P.E.P. §2131.

Furthermore, Mills instead discloses that MII one circuit 214 is for

communicating with a first collision domain 210 and that MII two circuit 216 is used for communicating with a second collision domain 212. Column 6, lines 60-63. The Examiner must provide a basis in fact and/or technical reasoning to support the assertion that a first and a second collision domain 210, 212, as disclosed in Mills, are collision recovery logic means. *Ex parte Levy*, 17 U.S.P.Q.2d 1461, 1464 (Bd. Pat. App. & Inter. 1990). That is, the Examiner must provide extrinsic evidence that must make clear that a first and a second collision domain 210, 212, as disclosed in Mills, are collision recovery logic means, and that it be so recognized for persons of ordinary skill. *In re Robertson*, 169 F.3d 743, 745, 49 U.S.P.Q.2d 1949, 1950-51 (Fed. Cir. 1999). Since the Examiner has not provided such evidence, the Examiner has not presented a *prima facie* case of anticipation in rejecting claim 1. M.P.E.P. § 2131.

Furthermore, Mills instead discloses that the 10 base T circuit 220 performs collision detection. Column 8, lines 9-13. Mills further discloses that the 100 base T circuit 230 performs collision detection. Column 8, lines 15-18. Hence, the 10 base T circuit 220 and the 100 base T circuit 230 (Examiner asserts that collectively the 10 base T circuit 220 and the 100 base T circuit 230 discloses a minimal number of generic interface signals) discloses collision detection and not collision recovery. Further, the Examiner must provide a basis in fact and/or technical reasoning to support the assertion that the 10 base T circuit 220 and the 100 base T circuit 230, as disclosed in Mills, are a minimal number of generic interface signals. *Ex parte Levy*, 17 U.S.P.Q.2d 1461, 1464 (Bd. Pat. App. & Inter. 1990). That is, the Examiner must provide extrinsic evidence that must make clear that the 10 base T circuit 220 and the 100 base T circuit 230, as disclosed in Mills, are a minimal number of generic interface signals, and that it be so recognized for persons of ordinary skill. *In re Robertson*, 169 F.3d 743, 745, 49 U.S.P.Q.2d 1949, 1950-51 (Fed. Cir. 1999). Since the Examiner has not provided such evidence, the Examiner has not presented a *prima facie* case of anticipation in rejecting claim 1. M.P.E.P. § 2131.

2. Claims 2-4 are not anticipated by Mills for at least the reasons that claim 1 is not anticipated by Mills.

Claims 2-4 recite the combinations of claim 1 and thus are not anticipated for at least the above-stated reasons as to why claim 1 is not anticipated by Mills.

3. Claim 8 is not anticipated by Mills.

Appellants respectfully assert that Mills does not disclose "at least two collision recovery means for providing collision recovery in the HPNA control chip according to at least two data rate standards" as recited in claim 8. The Examiner cites elements 210 and 212 as disclosing the two collision recovery means. Paper No. 5, page 8. Appellants respectfully traverse and assert that Mills instead discloses that MII one circuit 214 is for communicating with a first collision domain 210 and that MII two circuit 216 is used for communicating with a second collision domain 212. Column 6, lines 60-63. The Examiner must provide a basis in fact and/or technical reasoning to support the assertion that a first and a second collision domain 210, 212, as disclosed in Mills, are collision recovery logic means. *Ex parte Levy*, 17 U.S.P.Q.2d 1461, 1464 (Bd. Pat. App. & Inter. 1990). That is, the Examiner must provide extrinsic evidence that must make clear that a first and a second collision domain 210, 212, as disclosed in Mills, are collision recovery logic means, and that it be so recognized for persons of ordinary skill. *In re Robertson*, 169 F.3d 743, 745, 49 U.S.P.Q.2d 1949, 1950-51 (Fed. Cir. 1999). Since the Examiner has not provided such evidence, the Examiner has not presented a *prima facie* case of anticipation in rejecting claim 8. M.P.E.P. § 2131.

Appellants further assert that Mills does not disclose "a transmit data path logic means including a transmit state machine that interfaces with the at least two collision recovery means through a minimal number of generic interface signals" as recited in claim 8. As understood by the Appellants, the Examiner cites column 6,

lines 16-21 and column 7, lines 1-5 of Mills as disclosing the above-cited claim limitation. Paper No. 5, page 2. Appellants respectfully traverse. As stated above, Mills instead discloses a line driver/receiver circuit that is coupled to communicate information with a font end multiplexer circuit. Column 6, lines 16-18. Mills further discloses that the select input of the front end multiplexer circuit is controlled by a control signal in a bus generated by an auto-negotiation circuit. Column 6, lines 18-21. Mills further discloses that the select input of the back end multiplexer is controlled by the control bus that receives part of its signal from the result of the auto-negation circuit and part of its signal from a management interface circuit. Column 7, lines 1-5. There is no language in the cited passage that discloses a transmit data path logic means including a transmit state machine. Appellants performed a search of the phrase "state machine" in Mills and were unable to identify the phrase "state machine" or any variation thereof in Mills. Neither is there any language in the cited passage that discloses a transmit state machine that interfaces the transmit data path logic with at least two separate collision recovery means. Neither is there any language in the cited passage that discloses a transmit state machine that interfaces the transmit data path logic with at least two separate collision recovery means through a minimal number of generic interface signals. Thus, Mills does not disclose all of the limitations of claim 8, and thus Mills does not anticipate claim 8. M.P.E.P. §2131.

In response to the above argument, the Examiner cites element 250 of Mills as disclosing the transmit data path logic. Paper No. 5, page 7. The Examiner further cites elements 260 and 270 as well as column 6, lines 16-21 and column 7, lines 1-5 of Mills as disclosing a transmit state machine. Paper No. 5, page 7. The Examiner further cites column 6, lines 16-21 of Mills as disclosing interfacing the transmit data path logic. Paper No. 5, page 7. The Examiner further cites elements 210 and 212 as disclosing two collision recovery means. Paper No. 5, page 7. The Examiner further cites elements 220 and 230 as disclosing a minimal number of generic interface

signals. Paper No. 5, page 7. Appellants respectfully traverse the assertion that Mills discloses the above-cited claim limitation. Paper No. 5, page 7.

Mills instead discloses that the result of the auto-negotiation circuit 260 is used by the present invention to control both the front and back end multiplexers. Column 7, lines 13-16. Mills further discloses that auto-negotiation is performed between the auto-negotiation circuit 260 and an analogous auto-negotiation circuit 261 within adapter 280 in accordance with the IEEE 802.3 standard. Column 7, lines 16-19. Mills further discloses that the result of the auto-negotiation indicates whether adapter 280 supports 10 M or 100 M networking. Column 7, lines 19-21. Mills further discloses that the select input of the back end multiplexer is controlled by the control bus that receives part of its signal from the result of the auto-negotiation circuit and part of its signal from a management interface circuit 270. Column 7, lines 1-5. There is no language in Mills that discloses that the auto-negotiation circuit 260 and the management interface circuit 270 (Examiner asserts that elements 260 and 270 together disclose a transmit state machine) together interface the transmit data path logic (Examiner asserts that line driver/receiver 250 of Mills discloses a transmit data path logic) with at least two separate collision recovery means (Examiner asserts that elements 210 and 212 discloses collision recovery logic means) through a minimal number of generic interface signals. Instead, auto-negotiation circuit 260 performs auto-negotiation to indicate whether adapter 280 supports 10 M or 100 M networking. Further, Mills instead discloses that a signal is used from the management interface circuit 270 to control the back end multiplexer. Thus, Mills does not disclose all of the limitations of claim 8, and thus Mills does not anticipate claim 8. M.P.E.P. §2131.

Furthermore, Mills instead discloses that MII one circuit 214 is for communicating with a first collision domain 210 and that MII two circuit 216 is used for communicating with a second collision domain 212. Column 6, lines 60-63. The

Examiner must provide a basis in fact and/or technical reasoning to support the assertion that a first and a second collision domain 210, 212, as disclosed in Mills, are collision recovery means. *Ex parte Levy*, 17 U.S.P.Q.2d 1461, 1464 (Bd. Pat. App. & Inter. 1990). That is, the Examiner must provide extrinsic evidence that must make clear that a first and a second collision domain 210, 212, as disclosed in Mills, are collision recovery means, and that it be so recognized for persons of ordinary skill. *In re Robertson*, 169 F.3d 743, 745, 49 U.S.P.Q.2d 1949, 1950-51 (Fed. Cir. 1999). Since the Examiner has not provided such evidence, the Examiner has not presented a *prima facie* case of anticipation in rejecting claim 8. M.P.E.P. § 2131.

Furthermore, Mills instead discloses that the 10 base T circuit 220 performs collision detection. Column 8, lines 9-13. Mills further discloses that the 100 base T circuit 230 performs collision detection. Column 8, lines 15-18. Hence, the 10 base T circuit 220 and the 100 base T circuit 230 (Examiner asserts that collectively the 10 base T circuit 220 and the 100 base T circuit 230 discloses a minimal number of generic interface signals) discloses collision detection and not collision recovery. Further, the Examiner must provide a basis in fact and/or technical reasoning to support the assertion that the 10 base T circuit 220 and the 100 base T circuit 230, as disclosed in Mills, are a minimal number of generic interface signals. *Ex parte Levy*, 17 U.S.P.Q.2d 1461, 1464 (Bd. Pat. App. & Inter. 1990). That is, the Examiner must provide extrinsic evidence that must make clear that the 10 base T circuit 220 and the 100 base T circuit 230, as disclosed in Mills, are a minimal number of generic interface signals, and that it be so recognized for persons of ordinary skill. *In re Robertson*, 169 F.3d 743, 745, 49 U.S.P.Q.2d 1949, 1950-51 (Fed. Cir. 1999). Since the Examiner has not provided such evidence, the Examiner has not presented a *prima facie* case of anticipation in rejecting claim 8. M.P.E.P. § 2131.

4. Claims 9-11 are not anticipated by Mills for at least the reasons that claim 8 is not anticipated by Mills.

Claims 9-11 recite the combinations of claim 8 and thus are not anticipated for at least the above-stated reasons as to why claim 8 is not anticipated by Mills.

5. Claim 15 is not anticipated by Mills.

Appellants respectfully assert that Mills does not disclose "a physical layer (PHY)" as recited in claim 15. The Examiner cites to line driver/receiver circuit 250 of Mills as disclosing a physical layer (PHY). Paper No. 5, page 8. The Examiner had previously cited to line driver/receiver circuit 250 of Mills as disclosing a transmit data path logic. Paper No. 5, page 6. Based on the doctrine of claim differentiation, a transmit data path logic is not the same as a physical layer or else they would use the same term. The Examiner must cite to a different element as disclosing a physical layer. Thus, Mills does not disclose all of the limitations of claim 15, and thus Mills does not anticipate claim 15. M.P.E.P. §2131.

Further, in connection with the rejection of the above-cited claim limitation, the Examiner cites column 6, lines 16-21 of Mills as disclosing the above-cited claim limitation. Paper No. 5, page 8. Appellants respectfully traverse and assert that Mills instead discloses that the line driver/receiver circuit 250 is coupled to communicate information with a front end multiplexer circuit. Column 6, lines 16-18. Mills further discloses that the select input of the front end multiplexer circuit is controlled by a control signal in a bus generated by an auto-negotiation circuit. Column 6, lines 18-21. There is no language in the cited passage that discloses a physical layer. Thus, Mills does not disclose all of the limitations of claim 15, and thus Mills does not anticipate claim 15. M.P.E.P. §2131.

Furthermore, in connection with the rejection of the above-cited claim limitation, the Examiner asserts that the physical layer is present in order to transmit/receive data and cites three references to support such a proposition. Paper No. 5, pages 8-9. However, the Examiner is ignoring the claim language of claim 15.

Claim 15 recites a home phone networking alliance (HPNA) network control chip capable of collision recovery interface support that comprises a physical layer. The Examiner has to identify a single prior art reference that describes each and every element as set forth in claim 15. M.P.E.P. §2131. The Examiner has not provided a reference that discloses a home phone networking alliance (HPNA) network control chip capable of collision recovery interface support that comprises a physical layer. Thus, Mills does not disclose all of the limitations of claim 15, and thus Mills does not anticipate claim 15. M.P.E.P. §2131.

Appellants further assert that Mills does not disclose "the MAC further comprising at least two collision recovery means for providing collision recovery according to at least to two data rate standards, and a transmit data path logic means including a transmit state machine that interfaces with at least two collision recovery means through a minimal number of generic interface signals" as recited in claim 15. As understood by the Appellants, the Examiner cites column 6, lines 60-65 and column 7, lines 61-65 of Mills as disclosing the above-cited claim limitation. Paper No. 5, page 4. Appellants respectfully traverse and assert that Mills instead discloses that MII one circuit is for communicating with a first collision domain and MII two circuit is for communicating with a second collision domain. Column 6, lines 60-63. Mills further discloses that the switching functionality of the physical device can be controlled by the auto-negation circuit providing seamless switching between 100 M and 10 M domains without external switching circuitry. Column 7, lines 61-65. There is no language in the cited passages that discloses two collision recovery means for providing collision recovery according to at least to two data rate standards. Neither is there any language in the cited passages that discloses a transmit data path logic means that includes a transmit state machine. Neither is there any language in the cited passages that discloses a transmit data path logic means that includes a transmit state machine that interfaces with at least two collision recovery means. Neither is there any language in the cited passages that discloses a transmit data path

logic means that includes a transmit state machine that interfaces with at least two collision recovery means through a minimal number of generic interface signals. Thus, Mills does not disclose all of the limitations of claim 15, and thus Mills does not anticipate claim 15. M.P.E.P. §2131.

In response to Appellants' above argument, the Examiner cites elements 712 and 714 of Mills as disclosing a media access controller (MAC). Paper No. 5, page 9. The Examiner further cites elements 210 and 212 of Mills as disclosing collision recovery means. Paper No. 5, page 10. Appellants respectfully traverse. First, elements 210 and 212 (Examiner cites elements 210 and 212 as disclosing collision recover means) are not included within elements 712 and 714 (Examiner cites elements 712 and 714 as disclosing a MAC). Hence, the MAC 712 and 714 of Mills does not include elements 210 and 212 and thus Mills does not disclose a MAC that comprises at least two collision recovery means. Thus, Mills does not disclose all of the limitations of claim 15, and thus Mills does not anticipate claim 15. M.P.E.P. §2131.

Furthermore, Mills instead discloses that MII one circuit 214 is for communicating with a first collision domain 210 and that MII two circuit 216 is used for communicating with a second collision domain 212. Column 6, lines 60-63. The Examiner must provide a basis in fact and/or technical reasoning to support the assertion that a first and a second collision domain 210, 212, as disclosed in Mills, are collision recovery means. *Ex parte Levy*, 17 U.S.P.Q.2d 1461, 1464 (Bd. Pat. App. & Inter. 1990). That is, the Examiner must provide extrinsic evidence that must make clear that a first and a second collision domain 210, 212, as disclosed in Mills, are collision recovery means, and that it be so recognized for persons of ordinary skill. *In re Robertson*, 169 F.3d 743, 745, 49 U.S.P.Q.2d 1949, 1950-51 (Fed. Cir. 1999). Since the Examiner has not provided such evidence, the Examiner has not presented a *prima facie* case of anticipation in rejecting claim 15. M.P.E.P. § 2131.

6. Claims 2 and 9 are not anticipated by Mills.

Appellants respectfully assert that Mills does not disclose "wherein the minimal number of interface signals further comprises a GO signal from each separate collision recovery logic means" as recited in claim 2 and similarly in claim 9. The Examiner cites column 7, lines 61-65 of Mills as disclosing the above-cited claim limitation. Paper No. 5, page 3. Appellants respectfully traverse and assert that Mills instead discloses that the switching functionality of the physical device can be controlled by the auto-negation circuit providing seamless switching between 100 M and 10 M domains without external switching circuitry. Column 7, lines 61-65. There is no language in the cited passage that discloses that a minimal number of interface signals includes a GO signal. Neither is there any language in the cited passage that discloses that a minimal number of interface signals includes a GO signal from each separate collision recovery logic means (Examiner asserts that elements 210 and 212 of Mills disclose collision recovery logic means). Thus, Mills does not disclose all of the limitations of claims 2 and 9, and thus Mills does not anticipate claims 2 and 9. M.P.E.P. §2131.

In response to Appellants' above argument, the Examiner further cites to column 7, lines 10-35 of Mills as disclosing the above-cited claim limitation. Paper No. 5, page 10. Appellants respectfully traverse and assert that Mills instead discloses that the select input of the back end multiplexer is controlled by the control bus that receives part of its signal from the result of the auto-negotiation circuit and part of its signal from a management interface circuit 270. Column 7, lines 1-5. Mills further discloses that the result of the auto-negotiation circuit 260 is used by the present invention to control both the front and back end multiplexers. Column 7, lines 13-16. Mills further discloses that auto-negotiation is performed between the auto-negotiation circuit 260 and an analogous auto-negotiation circuit 261 within adapter 280 in accordance with the IEEE 802.3 standard. Column 7, lines 16-19.

Mills further discloses that the result of the auto-negotiation indicates whether adapter 280 supports 10 M or 100 M networking. Column 7, lines 19-21. There is no language in the cited passage that supports the Examiner's proposition on the bottom of page 10 and the top of page 11 of Paper No. 5. Neither is there any language that discloses a GO signal from each separate collision recovery logic means (Examiner asserts that elements 210 and 212 of Mills disclose collision recovery logic means). Thus, Mills does not disclose all of the limitations of claims 2 and 9, and thus Mills does not anticipate claims 2 and 9. M.P.E.P. §2131.

7. Claims 3 and 10 are not anticipated by Mills.

Appellants respectfully assert that Mills does not disclose "wherein the minimal number of interface signals further comprises a new transmit signal" as recited in claim 3 and similarly in claim 10. The Examiner cites column 7, lines 61-65 of Mills as disclosing the above-cited claim limitation. Paper No. 5, page 3. Appellants respectfully traverse and assert that Mills instead discloses that the switching functionality of the physical device can be controlled by the auto-negation circuit providing seamless switching between 100 M and 10 M domains without external switching circuitry. Column 7, lines 61-65. There is no language in the cited passage that discloses that a minimal number of interface signals includes a new transmit signal. Thus, Mills does not disclose all of the limitations of claims 3 and 10, and thus Mills does not anticipate claims 3 and 10. M.P.E.P. §2131.

In response to Appellants' above argument, the Examiner further cites to column 7, lines 10-35 of Mills as disclosing the above-cited claim limitation. Paper No. 5, page 10. Appellants respectfully traverse and assert that Mills instead discloses that the select input of the back end multiplexer is controlled by the control bus that receives part of its signal from the result of the auto-negotiation circuit and part of its signal from a management interface circuit 270. Column 7, lines 1-5.

Mills further discloses that the result of the auto-negotiation circuit 260 is used by the present invention to control both the front and back end multiplexers. Column 7, lines 13-16. Mills further discloses that auto-negotiation is performed between the auto-negotiation circuit 260 and an analogous auto-negotiation circuit 261 within adapter 280 in accordance with the IEEE 802.3 standard. Column 7, lines 16-19. Mills further discloses that the result of the auto-negotiation indicates whether adapter 280 supports 10 M or 100 M networking. Column 7, lines 19-21. There is no language in the cited passage that supports the Examiner's proposition on the bottom of page 10 and the top of page 11 of Paper No. 5. Neither is there any language that discloses a new transmit signal. Thus, Mills does not disclose all of the limitations of claims 3 and 10, and thus Mills does not anticipate claims 3 and 10. M.P.E.P. §2131.

8. Claims 4 and 11 are not anticipated by Mills.

Appellants respectfully assert that Mills does not disclose "wherein the minimal number of interface signals further comprises a transmit done signal" as recited in claim 4 and similarly in claim 11. The Examiner cites column 7, lines 61-65 of Mills as disclosing the above-cited claim limitation. Paper No. 5, page 3. Appellants respectfully traverse and assert that Mills instead discloses that the switching functionality of the physical device can be controlled by the auto-negation circuit providing seamless switching between 100 M and 10 M domains without external switching circuitry. Column 7, lines 61-65. There is no language in the cited passage that discloses that a minimal number of interface signals includes a transmit done signal. Thus, Mills does not disclose all of the limitations of claims 4 and 11, and thus Mills does not anticipate claims 4 and 11. M.P.E.P. §2131.

In response to Appellants' above argument, the Examiner further cites to column 7, lines 10-35 of Mills as disclosing the above-cited claim limitation. Paper No. 5, page 10. Appellants respectfully traverse and assert that Mills instead

discloses that the select input of the back end multiplexer is controlled by the control bus that receives part of its signal from the result of the auto-negotiation circuit and part of its signal from a management interface circuit 270. Column 7, lines 1-5. Mills further discloses that the result of the auto-negotiation circuit 260 is used by the present invention to control both the front and back end multiplexers. Column 7, lines 13-16. Mills further discloses that auto-negotiation is performed between the auto-negotiation circuit 260 and an analogous auto-negotiation circuit 261 within adapter 280 in accordance with the IEEE 802.3 standard. Column 7, lines 16-19. Mills further discloses that the result of the auto-negotiation indicates whether adapter 280 supports 10 M or 100 M networking. Column 7, lines 19-21. There is no language in the cited passage that supports the Examiner's proposition on the bottom of page 10 and the top of page 11 of Paper No. 5. Neither is there any language that discloses a transmit done signal. Thus, Mills does not disclose all of the limitations of claims 4 and 11, and thus Mills does not anticipate claims 4 and 11. M.P.E.P. §2131.

B. Claims 5-7, 12-14 and 16-18 are improperly rejected under 35 U.S.C. §103(a) as being unpatentable over Mills in view of Lu.

The Examiner has rejected claims 5-7, 12-14 and 16-18 under 35 U.S.C. § 103(a) as being unpatentable over Mills in view of Lu. Paper No. 5, page 4. Appellants respectfully traverse these rejections for at least the reasons stated below.

1. Mills and Lu, taken singly or in combination, do not teach or suggest claim 16.

Appellants respectfully assert that Mills and Lu, taken singly or in combination, do not teach or suggest "wherein the minimal number of interface signals further comprises a GO signal from each collision recovery means, a new transmit signal, a transmit done signal and a transmit priority indicator from the

transmit data" as recited in claim 16. The Examiner cites column 7, lines 61-65 of Mills as teaching all of the above-cited claim limitations except "transmit priority indicator from the transmit data." Paper No. 5, page 5. The Examiner further cites column 4, lines 52-56 of Lu as teaching the claim limitation of "transmit priority indicator from the transmit data." Paper No. 5, page 5. Appellants respectfully traverse.

As stated above, Mills instead teaches that the switching functionality of the physical device can be controlled by the auto-negation circuit providing seamless switching between 100 M and 10 M domains without external switching circuitry. Column 7, lines 61-65. There is no language in the cited passage that teaches that a minimal number of interface signals includes a GO signal. Neither is there any language in the cited passage that teaches that a minimal number of interface signals includes a GO signal from each separate collision recovery logic means. Neither is there any language in the cited passage that teaches that a minimal number of interface signals includes a new transmit signal. Neither is there any language in the cited passage that teaches that a minimal number of interface signals includes a transmit done signal. Therefore, the Examiner has not presented a *prima facie* case of obviousness in rejecting claim 16, since the Examiner is relying upon an incorrect, factual predicate in support of the rejection. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1455 (Fed. Cir. 1998).

Furthermore, as stated above, Lu instead teaches that in the home networking area, the Deference Algorithm module implements BEB on HPNA 1.0 or Ethernet 802.3 MAC, DFPQ on HPNA 2.0 and CSMA/CA and NAV on 802.11 MAC implementations. Column 4, lines 52-56. There is no language in the cited passage that teaches that a minimal number of interface signals includes a transmit priority indicator from the transmit data. Therefore, the Examiner has not presented a *prima facie* case of obviousness in rejecting claim 16, since the Examiner is relying upon an

incorrect, factual predicate in support of the rejection. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1455 (Fed. Cir. 1998).

2. Mills and Lu, taken singly or in combination, do not teach or suggest claims 6, 13 and 17.

Appellants respectfully assert that Mills and Lu, taken singly or in combination, do not teach or suggest "wherein the at least two separate collision recovery logic means further comprises a BEB collision recovery means" as recited in claim 6 and similarly in claims 13 and 17. The Examiner asserts that Mills teaches two separate collision recovery means. Paper No. 5, page 5. For at least the reasons stated above, Mills does not teach or suggest two separate collision recovery means. Therefore, the Examiner has not presented a *prima facie* case of obviousness in rejecting claims 6, 13 and 17, since the Examiner is relying upon an incorrect, factual predicate in support of the rejection. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1455 (Fed. Cir. 1998).

3. Mills and Lu, taken singly or in combination, do not teach or suggest claims 7, 14 and 18.

Appellants respectfully assert that Mills and Lu, taken singly or in combination, do not teach or suggest "wherein the at least two separate collision recovery logic means further comprises a DFPQ collision recovery means" as recited in claim 7 and similarly in claims 14 and 18. The Examiner cites column 4, lines 52-56 of Lu as teaching the above-cited claim limitation. Paper No. 5, page 6. Appellants respectfully traverse and assert that Lu instead teaches that the deference algorithm module implements DFPQ on HPNA 2.0. Column 4, lines 52-55. There is no language in the cited passage that teaches two separate collision recovery logic means. Neither is there any language in the cited passage that teaches two separate collision recovery logic means that includes a DFPQ collision recovery means.

Therefore, the Examiner has not presented a *prima facie* case of obviousness in rejecting claims 7, 14 and 18, since the Examiner is relying upon an incorrect, factual predicate in support of the rejection. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1455 (Fed. Cir. 1998).

4. The Examiner has not provided any objective evidence or appropriate motivation for modifying Mills with Lu and therefore claims 5, 6, 7, 12, 13, 14, 16, 17 and 18 are patentable over Mills in view of Lu.

Most if not all inventions arise from a combination of old elements. *See In re Rouffet*, 47 U.S.P.Q.2d 1453, 1457 (Fed. Cir. 1998). Obviousness is determined from the vantage point of a hypothetical person having ordinary skill in the art to which the patent pertains. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1457 (Fed. Cir. 1998). Therefore, an Examiner may often find every element of a claimed invention may often be found in the prior art. *Id.* However, identification in the prior art of each individual part claimed is insufficient to defeat patentability of the whole claimed invention. *See Id.* In order to establish a *prima facie* case of obviousness, the Examiner must show reasons that the skilled artisan, confronted with the same problems as the inventor and with no knowledge of the claimed invention, would select the elements from the cited prior art references for combination in the manner claimed. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1458 (Fed. Cir. 1998). That is, the Examiner must provide some suggestion or motivation, either in the references themselves, the knowledge of one of ordinary skill in the art, or, in some case, the nature of the problem to be solved, to modify the reference or to combine reference teachings. *See In re Dembiczak*, 175 F.3d 994, 999, 50 U.S.P.Q.2d 1614, 1617 (Fed. Cir. 1999). Whether the Examiner relies on an express or an implicit showing, the Examiner must provide particular findings related thereto. *In re Kotzab*, 55 U.S.P.Q.2d 1313, 1317 (Fed. Cir. 2000).

The Examiner admits that Mills does not teach the limitation of claims 5 and 12 ("wherein the minimal number of interface signals further comprises a transmit priority indicator from the transmit data"). Paper No. 5, page 4. The Examiner further admits that Mills does not teach "wherein the minimal number of interface signals further comprises....a transmit priority indicator from the transmit data" as recited in claim 16. Paper No. 5, page 5. The Examiner's motivation for modifying Mills with Lu to incorporate the above-cited claim limitations is "so as to provide a QOS guarantee at the physical layer (Lu, column 2, lines 17-29)." Paper No. 5, pages 4-5. The Examiner's motivation is insufficient to support a *prima facie* case of obviousness for at least the reasons stated below.

The Examiner's motivation ("to provide a QOS guarantee at the physical layer") does not provide reasons that the skilled artisan, confronted with the same problems as the inventor and with no knowledge of the claimed invention, would modify Mills to include the claim limitations of claims 5, 12 and 16. According, the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 5, 12 and 16. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1458 (Fed. Cir. 1998).

Mills addresses the problem of providing a low cost repeater hub that offers the flexibility of readily upgrading one or more ports of the hub to 100 M while allowing the remaining ports to operate at 10 M. Column 3, lines 41-44. The Examiner has not provided any reasons as to why one skilled in the art would modify Mills, which teaches providing a low cost repeater hub that offers the flexibility of readily upgrading one or more ports of the hub to 100 M while allowing the remaining ports to operate at 10 M, to include a transmit priority indicator from the transmit data or include a transmit priority indicator from the transmit data (Examiner admits that Mills does not teach these limitations). The Examiner's motivation ("to provide a QOS guarantee at the physical layer") does not provide such reasoning. The Examiner has not provided a rationale connection between providing a QOS

guarantee at the physical layer and including a transmit priority indicator from the transmit data or including a transmit priority indicator from the transmit data. The Examiner must provide objective evidence in modifying Mills to include the limitations of claims 5, 12 and 16. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002). Instead, the Examiner is merely relying upon his own subjective opinion which is insufficient to support a *prima facie* case of obviousness in rejecting claims 5, 12 and 16. *Id.* Consequently, the Examiner's motivation is insufficient to support a *prima facie* case of obviousness for rejecting claims 5, 12 and 16. *Id.*

In response to Appellants' above argument, the Examiner asserts that Appellants have admitted that the Examiner has provided a motivation for modifying Mills to include the limitations of claims 5, 12 and 16. Paper No. 5, page 11. The Examiner seems to be misunderstanding Appellants' argument. Appellants respectfully assert that the Examiner's stated motivation ("to provide a QOS guarantee at the physical layer") is insufficient to support a *prima facie* case of obviousness for rejecting claims 5, 12 and 16 for at least the reasons stated above.

Further, the Examiner admits that Mills does not teach the limitation of claims 6, 13 and 17 ("wherein the at least two separate collision recovery logic means further comprises a BEB collision recovery means"). Paper No. 5, page 5. The Examiner's motivation for modifying Mills with Lu to incorporate the above-cited claim limitations is "to defer its transmission when media is busy (Lu, column 2, lines 12-17)." Paper No. 5, page 5. The Examiner's motivation is insufficient to support a *prima facie* case of obviousness for at least the reasons stated below.

The Examiner's motivation ("to defer its transmission when media is busy") does not provide reasons that the skilled artisan, confronted with the same problems as the inventor and with no knowledge of the claimed invention, would modify Mills to include the claim limitations of claims 6, 13 and 17. According, the Examiner has

not presented a *prima facie* case of obviousness for rejecting claims 6, 13 and 17 *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1458 (Fed. Cir. 1998).

As stated above, Mills addresses the problem of providing a low cost repeater hub that offers the flexibility of readily upgrading one or more ports of the hub to 100 M while allowing the remaining ports to operate at 10 M. Column 3, lines 41-44. The Examiner has not provided any reasons as to why one skilled in the art would modify Mills, which teaches providing a low cost repeater hub that offers the flexibility of readily upgrading one or more ports of the hub to 100 M while allowing the remaining ports to operate at 10 M, to have at least two separate collision recovery logic means that includes a BEB collision recovery means (Examiner admits that Mills does not teach these limitations). The Examiner's motivation ("to defer its transmission when media is busy") does not provide such reasoning. The passage that the Examiner cited in Lu to support his motivation (column 2, lines 12-17) teaches a MAC that uses a binary exponential backoff algorithm to defer its transmission when the media is busy. The Examiner has not provided a rationale connection between a MAC using a binary exponential backoff algorithm to defer its transmission when the media is busy and having at least two separate collision recovery logic means include a BEB collision recovery means. The Examiner must provide objective evidence in modifying Mills to include the limitations of claims 6, 13 and 17. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002). Instead, the Examiner is merely relying upon his own subjective opinion which is insufficient to support a *prima facie* case of obviousness in rejecting claims 6, 13 and 17. *Id.* Consequently, the Examiner's motivation is insufficient to support a *prima facie* case of obviousness for rejecting claims 6, 13 and 17. *Id.*

In response to Appellants' above argument, the Examiner asserts that Appellants have admitted that the Examiner has provided a motivation for modifying Mills to include the limitations of claims 6, 13 and 17. Paper No. 5, page 12. The

Examiner seems to be misunderstanding Appellants' argument. Appellants respectfully assert that the Examiner's stated motivation ("to defer its transmission when media is busy") is insufficient to support a *prima facie* case of obviousness for rejecting claims 6, 13 and 17 for at least the reasons stated above.

Furthermore, the Examiner admits that Mills does not teach the limitation of claims 7, 14 and 18 ("wherein the at least two separate collision recovery logic means further comprises a DFPQ collision recovery means"). Paper No. 5, page 6. The Examiner's motivation for modifying Mills with Lu to incorporate the above-cited claim limitations is "so as to provide a QOS guarantee at the physical layer (Lu, column 2, lines 17-19)." Paper No. 5, page 13. The Examiner's motivation is insufficient to support a *prima facie* case of obviousness for at least the reasons stated below.

The Examiner's motivation ("to provide a QOS guarantee at the physical layer") does not provide reasons that the skilled artisan, confronted with the same problems as the inventor and with no knowledge of the claimed invention, would modify Mills to include the claim limitations of claims 7, 14 and 18. According, the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 7, 14 and 18. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1458 (Fed. Cir. 1998).

Mills addresses the problem of providing a low cost repeater hub that offers the flexibility of readily upgrading one or more ports of the hub to 100 M while allowing the remaining ports to operate at 10 M. Column 3, lines 41-44. The Examiner has not provided any reasons as to why one skilled in the art would modify Mills, which teaches providing a low cost repeater hub that offers the flexibility of readily upgrading one or more ports of the hub to 100 M while allowing the remaining ports to operate at 10 M, to have at least two separate collision recovery logic means include a DFPQ collision recovery means (Examiner admits that Mills

does not teach these limitations). The Examiner's motivation ("to provide a QOS guarantee at the physical layer") does not provide such reasoning. The Examiner has not provided a rationale connection between providing a QOS guarantee at the physical layer and having at least two separate collision recovery logic means include a DFPQ collision recovery means. The Examiner must provide objective evidence in modifying Mills to include the limitations of claims 7, 14 and 18. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002). Instead, the Examiner is merely relying upon his own subjective opinion which is insufficient to support a *prima facie* case of obviousness in rejecting claims 7, 14 and 18. *Id.* Consequently, the Examiner's motivation is insufficient to support a *prima facie* case of obviousness for rejecting claims 7, 14 and 18. *Id.*

VIII. CONCLUSION

For the reasons noted above, the rejections of claims 1-18 are in error. Appellants respectfully request reversal of the rejections and allowance of claims 1-18.

Respectfully submitted,

WINSTEAD SECHREST & MINICK P.C.

Attorneys for Appellants

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(512) 370-2832

CLAIMS APPENDIX

1. A method for collision recovery interface support in a home phoneline networking alliance (HPNA) control chip, the method comprising the steps:

(a) providing transmit data path logic to receive and transmit data packets within the HPNA control chip; and

(b) consolidating the transmit data path logic to include a transmit state machine that handles interfacing the transmit data path logic to at least two separate collision recovery logic means of the HPNA control chip through a minimal number of generic interface signals.

2. The method of claim 1 wherein the minimal number of interface signals further comprises a GO signal from each separate collision recovery logic means.

3. The method of claim 2 wherein the minimal number of interface signals further comprises a new transmit signal.

4. The method of claim 3 wherein the minimal number of interface signals further comprises a transmit done signal.

5. The method of claim 4 wherein the minimal number of interface signals further comprises a transmit priority indicator from the transmit data.

6. The method of claim 1 wherein the at least two separate collision recovery logic means further comprises a BEB collision recovery means.

7. The method of claim 6 wherein the at least two separate collision recovery logic means further comprises a DFPQ collision recovery means.

8. A system for collision recovery interface support in a home phoneline

networking alliance (HPNA) control chip, the system comprising:

at least two collision recovery means for providing collision recovery in the HPNA control chip according to at least two data rate standards; and

a transmit data path logic means including a transmit state machine that interfaces with the at least two collision recovery means through a minimal number of generic interface signals.

9. The system of claim 8 wherein the minimal number of interface signals further comprises a GO signal from each collision recovery means.

10. The system of claim 9 wherein the minimal number of interface signals further comprises a new transmit signal.

11. The system of claim 10 wherein the minimal number of interface signals further comprises a transmit done signal.

12. The system of claim 11 wherein the minimal number of interface signals further comprises a transmit priority indicator from the transmit data.

13. The system of claim 8 wherein the at least two collision recovery means further comprises a BEB collision recovery means.

14. The system of claim 13 wherein the at least two collision recovery means further comprises a DFPQ collision recovery means.

15. A home phone networking alliance (HPNA) network control chip capable of collision recovery interface support, the chip comprising:

a media independent interface (MII);

a physical layer (PHY); and

a media access control (MAC) coupled between the MII and the PHY, the MAC further comprising at least two collision recovery means for providing collision recovery according to at least two data rate standards, and a transmit data path logic means including a transmit state machine that interfaces with the at least two collision recovery means through a minimal number of generic interface signals.

16. The method of claim 15 wherein the minimal number of interface signals further comprises a GO signal from each collision recovery means, a new transmit signal, a transmit done signal, and a transmit priority indicator from the transmit data.

17. The method of claim 15 wherein the at least two collision recovery means further comprises a BEB collision recovery means.

18. The method of claim 17 wherein the at least two collision recovery means further comprises a DFPQ collision recovery means.

EVIDENCE APPENDIX

No evidence was submitted pursuant to §§1.130, 1.131, or 1.132 of 37 C.F.R. or of any other evidence entered by the Examiner and relied upon by Appellants in the Appeal.

RELATED PROCEEDINGS APPENDIX

There are no related proceedings to the current proceeding.

PTO/SB/21 (09-04)
Approved for use through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Total Number of Pages in This Submission	39

Application Number	09/893,100
Filing Date	06/26/2001
First Named Inventor	Peter Chow
Art Unit	2661
Examiner Name	Andrew W. Wahba
Attorney Docket Number	F0999

ENCLOSURES *(Check all that apply)*

- [✓] Fee Transmittal Form
  - [ ] Fee Attached
- [ ] Amendment/Reply
  - [ ] After Final
  - [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
- [ ] Certified Copy of Priority Document(s)
- [ ] Reply to Missing Parts/ Incomplete Application
  - [ ] Reply to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Drawing(s)
- [ ] Licensing-related Papers
- [ ] Petition
- [ ] Petition to Convert to a Provisional Application
- [ ] Power of Attorney, Revocation Change of Correspondence Address
- [ ] Terminal Disclaimer
- [ ] Request for Refund
- [ ] CD, Number of CD(s) _____
  - [ ] Landscape Table on CD
- [ ] After Allowance Communication to TC
- [ ] Appeal Communication to Board of Appeals and Interferences
- [✓] Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
- [ ] Proprietary Information
- [ ] Status Letter
- [✓] Other Enclosure(s) (please Identify below):
  Return Postcard

Remarks

Amended Supplemental Appeal Brief

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	Winstead Sechrest & Minick P.C.		
Signature			
Printed name	Robert A. Voigt, Jr.		
Date	12/06/2005	Reg. No.	47,159

CERTIFICATE OF TRANSMISSION/MAILING

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Signature	Toni Stanley		
Typed or printed name	Toni Stanley	Date	12/06/2005

PTO/SB/17 (11-04)
Approved for use through 07/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Effective on 10/01/2004. Patent fees are subject to annual revision.

FEE TRANSMITTAL
For FY 2005

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) **500.00**

Complete if Known	
Application Number	09/893,100
Filing Date	06/26/2001
First Named Inventor	Peter Chow
Examiner Name	Andrew W. Wahba
Art Unit	2661
Attorney Docket No.	F0999

METHOD OF PAYMENT (check all that apply)

☐ Check ☐ Credit Card ☐ Money Order

☑ Deposit Account ☐ None

Deposit Account Number: 01-0365

Deposit Account Name: Advanced Micro Devices, Inc.

The Director is hereby authorized to: (check all that apply)

☑ Charge fee(s) indicated below

☐ Charge fee(s) indicated below, **except for the filing fee**

☑ Charge any additional fee(s) or underpayments of fee(s) under 37 CFR 1.16 and 1.17

☑ Credit any overpayments

to the above-identified deposit account.

☐ Other (please identify): _____

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FEE CALCULATION

1. BASIC FILING FEE

Fee Description	Fee ($)	Small Entity Fee ($)	Fee Paid($)
Utility Filing Fee	790	395	
Design Filing Fee	350	175	
Plant Filing Fee	550	275	
Reissue Filing Fee	790	395	
Provisional Filing Fee	160	80	

Subtotal (1) $ _____

FEE CALCULATION (continued)

2. EXTRA CLAIM FEES

Fee Description	Fee ($)	Small Entity Fee ($)
Each claim over 20	50	25
Each independent claim over 3	200	100
Multiple dependent claims	360	180
For Reissues, each claim over 20 and more than in the original patent	50	25
For Reissues, each independent claim more than in the original patent	200	100

Total Claims	Extra Claims	Fee ($)	Fee Paid ($)
_____ - 20 or HP =	_____	x _____	= _____

HP = highest number of total claims paid for, if greater than 20

Indep. Claims	Extra Claims	Fee ($)	Fee Paid ($)
_____ - 3 or HP =	_____	x _____	= _____

HP = highest number of independent claims paid for, if greater than 3

Multiple Dependent Claims	Fee ($)	Fee Paid ($)
	_____	_____

Subtotal (2) $ _____

3. OTHER FEES

Fee Description	Fee ($)	Small Entity Fee ($)	Fee Paid($)
1-month extension of time	120	60	
2-month extension of time	450	225	
3-month extension of time	1,020	510	
4-month extension of time	1,590	795	
5-month extension of time	2,160	1,080	
Information disclosure stmt. fee	180	180	
37 CFR 1.17(q) processing fee	50	50	
Non-English specification	130	130	
Notice of Appeal	500	250	
Filing a brief in support of appeal	500	250	500
Request for oral hearing	1,000	500	
Other: _____			

Subtotal (3) $ 500.00

SUBMITTED BY

Signature		Registration No. (Attorney/Agent) 47.159	Telephone 512.370.2832
Name (Print/Type)	Robert A. Voigt, Jr.		Date 12/06/2005